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Development of Low Power Test Data Compression Techniques for Digital VLSI Circuits

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Abstract: The two noteworthy zones of worry in the testing of VLSI circuits are Test data volume and inordinate test control. Among the various pressure coding plans proposed till now, the CCSDS (Consultative Committee for Space Data Systems) lossless data pressure plan is one of the best. This paper talks about the procedures that test data pressure conspire in view of lossless data pressure Rice Algorithm as suggested by the CCSDS for the lessening of required test data add up to be put away on the analyzer, which will be exchanged amid assembling testing to every center in a system-on-a-chip (SOC). In the proposed plot, the test vectors for the SOC are compacted by utilizing Rice Algorithm, and by applying different parallel encoding methods. Exploratory results demonstrate that the test data pressure proportion for the bigger ISCAS 89 Benchmark Circuits is altogether enhanced in examination with existing techniques.

Keywords: VLSI Circuits, CCSDS, SOC, Adaptive Entropy Coder (AEC).

I. INTRODUCTION

It is truly hard to test advanced circuits as a cumbersome measure of test information must be conveyed to the circuit under test (CUT). It is harder to test VLSI chips, in light of their muddled usefulness and size brought on by expanded coordination levels of VLSI chips. Moreover, testing of VLSI outline is entirely costly. In this way, VLSI makers go for diminishing the test cost of these circuits. The two imperative variables adding to test cost are the test information volume and test control. While testing SOCs, the hardest errand is taking care of the immense measure of test information that must be exchanged between the analyzer and the chip. Arrangements of test vectors are available in every center of a SOC that ought to be connected to the center. Amid secluded testing, it is important to store these test vectors on an analyzer and after that exchange them to the contributions of the center. This causes a major issue in light of the expensiveness negative marks of robotized test hardware (ATE). Analyzers have restricted speed, memory and channel limit.

II. REVIEW OF LITERATURE

Robert F. Rice from NASA built up the Rice Coding whereupon the CCSDS [1] standard depends on. A lossless source coding strategy monitors source information precision and takes out repetition in the information source. The lossless Rice coder has two distinctive utilitarian parts, viz., the preprocessor and the versatile entropy coder its appeared in figure1. The execution measure in the coding bit rate (bits per test) of a lossless information pressure method relies on upon two imperative variables. They are the measure of relationship dispensed with among information tests the preprocessing stage, and the coding productivity of the entropy coder. The pre processor capacities in de-associating information and reformatting them into non-negative numbers with the favored likelihood dispersion. The coding alternative that plays out the best on the present square of tests is chosen by the Adaptive Entropy Coder (AEC). The code determination depends on the quantity of bits that the chose choice will use to code the present piece of tests. An ID bit grouping will indicate the choice used to encode the going with set of code words.

According to Moore's, the number of transistors integrated per square inch on a die has doubled every year and half since the integrated circuit was invented. Also, every few years the size of the transistors employed is shrunken and the frequency of circuits increases. As these trends continue, several new challenges become relevant in the testing of very-large-scale-integrated (VLSI) circuits. With the advance of semiconductor manufacturing technology, the requirements of digital VLSI circuits have led to many challenges during manufacturing test. This is because of

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the large and complex chips which require a huge amount of test data and dissipate a substantial amount of power during test, resulting in considerable increases in test cost.

III. OBJECTIVE OF STUDY

With the regularly expanding coordination ability of semiconductor innovation, today's extensive incorporated circuits requires an expanding measure of information for testing which builds test time and raised necessities of analyzer memory. Bigger test information sizes request high memory necessities, as well as an immense increment in the testing time. These remain the bottleneck for testing the entire framework

i. To Study the High-Power Utilization Amid: This fragment delineates the reason behind high-control usage in the midst of test. There are a couple of clarifications behind high test control. The standard reasons are, in the test mode, the exchanging movement of all hubs is few times higher than the exchanging action in the midst of regular operation. In a SoC, parallel testing is a significant part of the time performed to lessen the test time, which may construct power and vitality dissemination. Input vector connected to a given circuit has basic relationship in the midst of framework mode, while the progressive test designs have low relationship. This prompts bigger exchanging action and power dispersal in circuit in the midst of test than amid its normal operation. To decrease the test complex trouble, the plan for-testability hardware is profoundly set encompassed by and some portion of circuit. It is by and large futile amid run of the mill operations however may be genuinely used as a part of the test mode.

ii. To Demonstrate Low-Power X-Filling: As a portion of the test vectors are left with unspecified esteem; for instance 10X01X. In X filling procedure every X bit is supplanted by 0 or 1. The principle indicates is diminishing the quantity of move in sweep cell which prompts to the lessening in general exchanging. The X filling strategy is isolated into three diverse methodologies: least move filling system (MT-filling), 0 filling (set all X bit to 0), 1 filling (set all X bit to 1) .As a straightforward case, consider the test 3D shape [0XX1X0X1XX]. By applying every one of the three filling systems on above test tube the subsequent vectors and the quantity of moves will be

- MT-Filling: 0001100111 (3 transitions)
- 0-Filling: 0001000100 (4 transitions)
- 1-Filling: 0111101111 (3 transitions)

IV. SCOPE OF THE STUDY

i. To Test Vector Requesting Methods: The exploration has extensively researched the test vector reordering techniques to decrease the exchanging power. Hamming separation based reordering [3] for pressure of test information. Advantage of this strategy is an exclusive requirement pressure with low test control finished without including territory overhead. Artificial insight based strategy [4] orders the test vectors in a perfect approach abatement exchanging movement amid testing.

ii. To Diminish The Transitions: These systems reduce the moves between back to back examples delivered by LFSR and what's more between the progressive bits in a given example. A double speed LFSR arrange [5] relies on upon two particular speed LFSRs to lessen the circuit's general internal overall activity by interfacing inputs that have raised move densities to the direct speed LFSR. This technique in a general sense reduces the normal power and vitality use without decreasing shortcoming scope. Cell mechanized based test design generators [6] effectively diminish control usage while finishing high blame scope. In weighted arbitrary example testing, the LFSR is modified by including weight sets to tune the pseudorandom vectors flag probabilities and as a consequence of that lessen vitality usage and extend the blame scope. The LP-TPG insert middle examples between the irregular examples to reduce the transitional exercises of essential information sources which over the long haul diminishes the exchanging exercises inside the circuit under test, and subsequently, control use. Extraordinary failure control BIST TPG arrange uses a move checking window (TMW) that incorporates a TMW square and a MUX. This technique quells the moves of examples using the k-esteem which is a standard that is gotten from the transport of TMW to analyze over transitive examples realizing high-control scattering in an output chain. A low equipment overhead test design generator (TPG) for output based Built-In Self-Test (BIST) that can lessen exchanging movement in circuits under tests (CUTs) during BIST. It similarly finishes high blame scope with sensible lengths of test arrangements. BIST TPG reduces moves that happen at sweep contributions in the midst of output move operations and therefore decreases exchanging action in the CUT. In LT-LFSR moves in LFSR are diminished in two estimations: (i) between progressive examples and (ii) between serial bits. A low-control dynamic LFSR circuit finishes comparable execution with less power usage.

V. RESEARCH METHODOLOGY

The experimental results for the various ISCAS89 benchmark circuits test vectors are compressed and presented in the following table. We have used the Mintest [2] test data .We achieved the highest compression percentage for the different benchmark circuits. The comparison is also given in the table below

Compression Efficiency (%)				
Circuits	Golomb 11	Selective Huffman	FDR	RICE
s9234	45	54	61	74.1622
s13207	80	30	88	92.01
s38417	28	45	66	91.00

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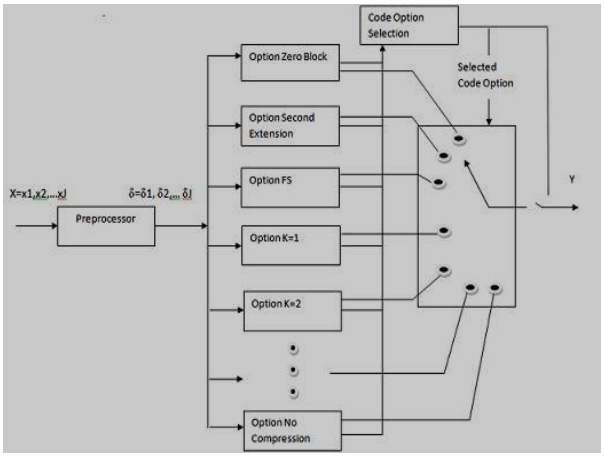
i. Compression Method: Test vectors are compacted utilizing Rice entropy coding [1]. The entropy coder first changes over the quantity of input vectors xi into preprocessor tests utilizing indicator. The preprocessing is done utilizing an indicator, and at that point by an expectation blunder mapper. In view of the anticipated esteem, the expectation blunder mapper changes over each expectation to error and bit non negative value, integer, which is appropriate for handling by the entropy coder. For instance, the benchmark circuit S298 Vectors are taken, and the indicator is connected to 8 bit information values from 0 to 255, as demonstrated as follows.



ii. Low-Power Test Pattern Generation: Test design era is primary piece of testing circuits by which exchanging movement can be diminished. Power can be decrease amid testing by low power test compaction, low power X-filling, and test vector ordering. With the offer assistance of this strategy two issues, similar to circuit overheat and execution corruption can be overcome.

iii. Low Power Test Compaction: The prerequisite of compaction is to diminish number of test vectors. Test 3D shape can be abused utilizing test compaction; test 3D shapes are the test vector containing unspecified bits or X-bits. Test information compaction should be possible as dynamic compaction and static compaction. Dynamic compaction determines the X-bits in a test solid shape keeping in mind the end goal to distinguish a bigger number of issues than the at first focused on blame, while static compaction utilizes the X - bits in perfect test 3D squares to union them into one test 3D square.

iv. Artificial Intelligence Approach to Test Vector Reordering: With the assistance of this method we can beat the issues like unwavering quality and fleeting glitch. In this system, we have decreased element control utilization amid test application without losing stuck to blame scope.

v. Scan Chain Reordering: Utilizing examines chain reordering the general normal power and pinnacle power is decreased. In this strategy blame scope, test application time, and equipment territory overhead is immaterial.

VI. CONCLUSION

Rice Algorithm coding is an extraordinary approach to pack test information. It accompanies double advantages in that, it lessens both the measure of test information required to be put away on the analyzer and the time taken to exchange the test information from the analyzer to the CUT. In this paper, we have talked about of how we have connected our calculation on various benchmark circuits, and have made correlation of our outcomes with existing test pressure procedures.

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